LINEAR VOLTAGE SUBTRACTOR/ADDER CIRCUIT AND MOS DIFFERENTIAL AMPLIFIER CIRCUIT THEREFOR

Abstract of the Disclosure

A voltage subtractor/adder circuit comprises a differential pair having first and second MOS transistors. Gate electrodes of the first and second MOS transistors form input terminals for receiving an input differential voltage. Drain electrodes of the first and second MOS transistors form output terminals for outputting a subtraction output signal. Source electrodes of the first and second MOS transistors are commonly coupled to form an output terminal for addition output voltage. The sum of currents flowing through the first and second MOS transistors increases in proportion to the square of the input differential voltage. It is also possible to drive the differential pair by a constant current source. A level shifter may be provided for level-shifting the addition output voltage from the commonly coupled source electrodes.